Resonance-based Optimized Buck LED Driver Using Unequal Turn Ratio Coupled Inductance

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***Abstract*- Losses in light-emitting-diode (LED) driver cause increasing temperature and shorten their lifespan. Therefore, improving the efficiency of LED drivers not only saves energy but also is indispensable to increase their lifespan. In this study, a new LED driver topology is proposed to improve the performance of valley switching by decreasing the MOSFET switching losses. The proposed topology is designed in a way that the MOSFET works at the significantly lower switching and conduction losses in compared with conventional LED drivers. It elaborates how the proposed topology also improves the overall efficiency by decreasing power losses in other main elements of the driver including inductance, and diode. In addition, a new valley switching implementation is introduced for the new converter which decreases the cost and dimension of the LED drivers. The experimental results confirm the high efficient operation of the proposed LED driver by reaching the efficiency up to 97% at a wide range of operating voltage.**

***Index Terms*--- Buck LED driver, high efficient LED driver, low output voltage, valley switching.**

I. INTRODUCTION

Today incandescent and fluorescent lamps are replaced by LED lamps due to their long lifespan, non-mercury content, high efficiency, and simple control. A lot of researches investigated different aspects of these lamps to increase their controllability, efficiency, lifespan, and performance. These lamps need a driver to supply constant voltage or current. Different converter topologies such as buck, boost, buck-boost, flyback are used as LED driver. These converter uses pulse width modulation (PWM) technique to control the output current and voltage; as a result, the output current has ripple and the lamp has flicker. In this view, some studies focused on mitigating the output current ripple and attenuating the flicker [1]-[3]. Most of converters use a diode bridge and an electrolytic capacitor to supply the LED lamp. Some researches tried to eliminate the input bridge using new control method and novel LED driver [4]-[5]. However, using electrolytic capacitors at the input of these converter shorten their lifespan; therefore, some researches tried to improve the lifespan of LED lamp by eliminating these bulk capacitor [6]-[11]. Poor power factor is another problem of these lamps which causes using power factor correction (PFC) converter for LED driver. However, using PFC converter increase the overall cost of LED lamp. Thus, some studies attempted to overcome this drawback by combining PFC converter and LED driver in a single converter [12]-[15]. Although LED lamps have higher efficiency in compared with other lamps, power losses in LED drivers cause rising temperature which results in shortening their lifespan. Therefore, thermal management and preventing power loss in LED drivers are indispensable to control their temperature and improving LED's efficiency [16]. These losses are mainly included losses in converter inductance, diodes, input bridge, and losses in the MOSFET switching and conduction [17]. Zero voltage switching (ZVS) and zero current switching (ZCS) are implemented using resonance phenomena to decrease the switching losses and increase the efficiency [18]-[24]. However, extra circuit elements such as capacitors and inductors are required to implement the resonance which increases the size and overall cost issues. Valley switching method is a solution for these issues which uses the resonance between the converter inductance and parasitic output capacitance of the MOSFET instead of extra circuit elements [25]-[28]. However, the minimum point of resonance voltage is not low enough to decrease the switching losses sufficiently in low output voltage; therefore, using resonance in this condition is not efficient. In this paper, a new topology is proposed to minimize the valley point of resonance at the MOSFET output voltage to zero, so that the MOSFET switching losses minimized at this point. Also, it shows that the new topology decreases the conduction losses of the MOSFET in addition to switching losses. Besides decreasing the MOSFET losses, the other elements' losses such as inductor and diode conduction losses and input bridge losses are decreased, significantly. In this proposed topology, the implementation of valley switching without requiring a secondary winding makes an LED driver more efficient and cheaper in compared with other designs in which a secondary winding coupled by the converter inductance is required to detect the minimum point of the MOSFET output voltage [27]. Accordingly, the contributions of this paper can be summarized as:

1- A new high efficient buck LED driver is introduced and its output current and voltage relation to the input reference current and input voltage is achieved. In addition, all main element losses analyzed and illustrated by equations and figures.

2- A new valley switching is introduced according to the new topology which is implemented more easily and cost-effective.

The rest of the paper is organized as follows. In section II, valley switching in buck LED drivers is explained. Section III elaborates the operation of the proposed LED driver while in Section IV the efficiency of the proposed topology is

compared with the conventional buck LED driver. In Section V, the implementation of new valley switching is represented. The experimental results of the proposed topology are shown in Section VI. Finally, the conclusions are drawn in Section VII.

II. Valley Switching in Buck LED Drivers

Fig. 1 shows conventional buck LED driver in which the MOSFET is placed in the low voltage side. Valley switching method uses resonance between converter inductance (L) and parasitic output capacitance of MOSFET (C_{oss}) to decrease the switching losses. The MOSFET output capacitance and its body diode and the converter inductance are shown in red color to emphasis the main resonance elements. Fig. 2 shows the inductance current and the MOSFET output voltage in current control mode and valley switching control. As can be seen, the inductance current rises to maximum reference current (I_{max}) when the MOSFET turns on, and then the MOSFET turns off and the inductance current falls to zero. A resonance is occurred at this moment between the converter inductance and parasitic output capacitance of the MOSFET (point **a**). The MOSFET turns on when the output voltage of the MOSFET reaches its minimum value or zero (point **b**). The output voltage equation of the MOSFET (v_Q) and the inductance current depend on input voltage value (V_{in}) and output voltage value (V_o). There are two cases. A full resonance oscillation is occurred when the input voltage value is greater than $2V_o$ while in the other case, the output voltage of MOSFET tends to be a negative value at T_m; therefore, the body diode of the MOSFET turns on and output voltage clamps to zero. Equations (1) shows the output voltage of the MOSFET ($v_Q(t)$) for these two cases where the reonant angular frequency (ω) is represented by (2).

$$v_Q(t)=\begin{cases}\begin{cases}(V_{in}-V_o)+V_o\cos(\omega t) & t\le T_m\\ 0 & t>T_m\end{cases} & V_{in}<2V_o\\ (V_{in}-V_o)+V_o\cos(\omega t) & V_{in}\ge 2V_o\end{cases} \tag{1}$$

$$\omega=\frac{1}{\sqrt{LC_{oss}}} \tag{2}$$

The output voltage of the conventional converter can be achived by inductance volt-second method.

$$V_o=D_{CC}V_{in} \tag{3}$$

where D_{CC} is duty cycle of the conventional converter. The on state switching losses depend on input voltage and output voltage values as shown in (4).

$$P_{swON}=\begin{cases}0.5f_{sw}C_{oss}(V_{in}-2V_o)^2 & V_{in}\ge 2V_o\\ 0 & V_{in}<2V_o\end{cases} \tag{4}$$

where P_{swON} and f_{sw} are on state switching losses and switching frequency, respectively. Equation (4) indicates that switching losses increase in applications where the output voltage value is low.

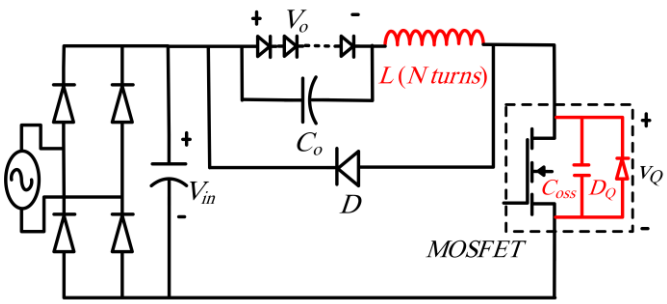

Fig. 1. Conventional buck LED driver.

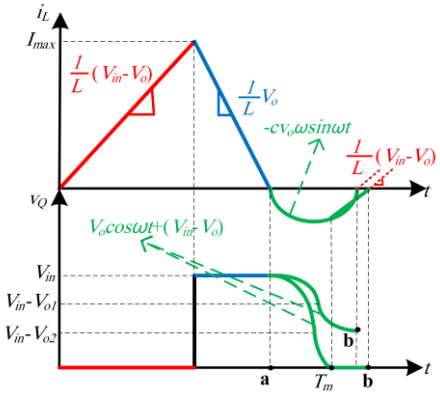

Fig. 2. Inductance current and the MOSFET output voltage (Red, blue, and green color are signals related to the on state switching, off state switching, and resonance, respectively).

III. Operation of the Proposed LED Driver

Minimum value of the MOSFET's voltage is (V_{in}-$2V_o$) according to (1); therefore, the switching losses increase in low output voltage, consequently the valley switching is not efficient for this application. Fig 3 shows the proposed buck LED driver to overcome the high switching losses in low output voltage. In this converter, zero voltage switching (ZVS) is achieved together with zero current switching (ZCS) when valley switching is activated. Here in this configuration, the converter inductance (L), previously shown in Fig. 1 with N turns, is divided into two inductances with N_1 and N_2 turns which are wound on a core to build coupled windings. As shown in (5), the winding turn ratio (n) of these inductances is equal or greater than the ratio of input voltage to output voltage values subtracted by 2.

$$n=\frac{N_2}{N_1}\ge\left(\frac{V_{in}}{V_o}-2\right). \tag{5}$$

Note that the secondary winding turns are higher than the primary turns and as shown in Fig. 3 an auxiliary capacitor (C_{ax}) and a diode (D_2) are connected to it. In this configuration, the secondary voltage becomes equal to the output voltage value (V_o) in off state of the MOSFET if this capacitor is emitted, therefore the primary voltage value becomes lower than the output voltage. In this condition, the diode D_1 is backward biased and it never turns on. This capacitor prevents diode D_2 from conducting in off state of the MOSFET.

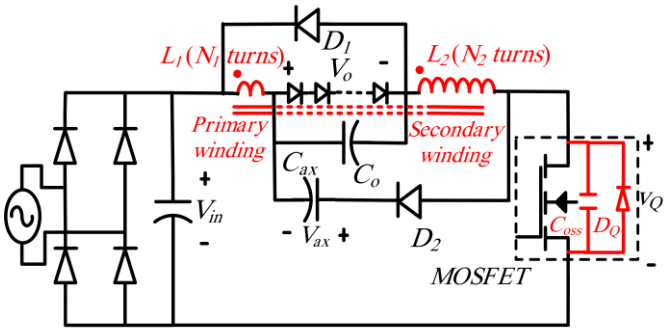

Fig. 3. The propose buck LED driver.

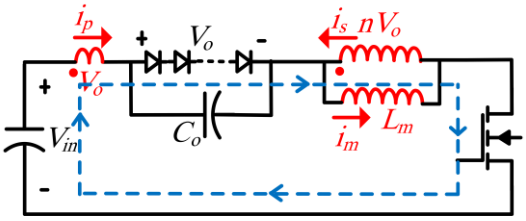

Fig. 4. The proposed circuit in MOSFET on state.

The reason is that since there is not any load parallel to C_2, its average current is not zero and its voltage becomes greater than nV_o and in this moment the D_2 becomes backward biased, therefore only diode D_1 conducts when the MOSFET turns off. Fig. 4 shows the driver when the MOSFET is in on state. In this figure, the transformer model of coupling inductance is used. Note that because leakage inductances do not affect the circuit operation, they are not shown for simplicity in illustration. Similarly, diodes D_1 and D_2 are backward biased in this state, therefore they are not included in this figure. Primary current of transformer is the load current of the converter which can calculated by (6) where i_p, i_s, and i_m are the primary, secondary and magnetizing current of the transformer, respectively.

$$\left.\begin{aligned} & i_p = n i_s \\ & i_m = i_s + i_p = \frac{n+1}{n} i_p \\ & v_{Lm} = \frac{n}{n+1}\left(V_{in} - V_o\right) \end{aligned}\right\} \Rightarrow i_p(t) = \frac{1}{L_m}\left(\frac{n}{n+1}\right)^2 \left(V_{in} - V_o\right) t \quad (6)$$

where L_m is the magnetizing inductance of the transformer. In current control mode, the MOSFET turns off when the output current reaches to a predetermined maximum reference value (I_{NCmax}). Fig. 5 shows transformer model of inductance and emits elements which do not affect the operation when the MOSFET is in off state. In steady state, when the MOSFET turns off, only diode D_1 conducts and resets the magnetizing inductance energy and diode D_2 does not conduct. In real application and non-ideal inductance, diode D_2 discharges the leakage inductance energy of secondary winding (l_{l2}). The output current can be calculated by (7).

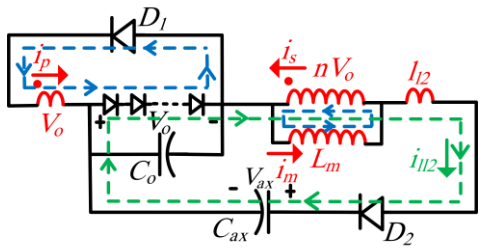

Fig. 5. The proposed circuit in MOSFET off state.

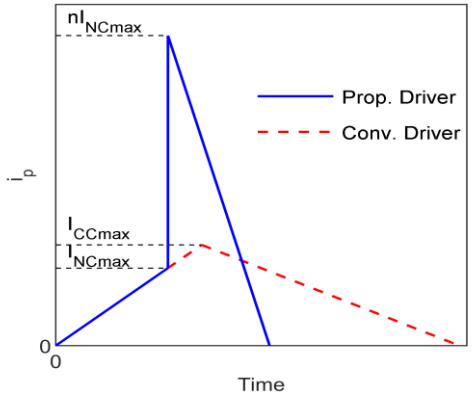

Fig. 6. Theoretical waveform of inductance current for the conventional and the proposed converter.

$$\left.\begin{aligned} & i_p = n i_s \\ & i_m = i_s = \frac{1}{n} i_p \\ & v_{Lm} = -n V_o \\ & i_m = I_{NC\max} + \frac{1}{L_m} V_{Lm} t \end{aligned}\right\} \Rightarrow i_p(t) = n I_{NC\max} - \frac{1}{L_m} n^2 V_o\, t \quad (7)$$

Fig. 6 shows the output current of the proposed current according to (6) and (7). The average output current can be calculated using the primary current.

$$I_{NCave} = \frac{1}{2}\left(D_{NC} + n\left(1 - D_{NC}\right)\right) I_{NC\max} \quad (8)$$

where I_{NCave} and D_{NC} are average current and duty cycle of the proposed converter, respectively. This current for conventional converter is:

$$I_{CCave} = \frac{1}{2} I_{CC\max} \quad (9)$$

where I_{CCave}, and I_{CCmax} are the average, and maximum current of the conventional converter. The steady state output voltage value (10) and auxiliary capacitors voltage value (11) can be calculated using voltage second of inductor.

$$V_o = \frac{D_{NC}}{D_{NC} + (n+1)(1 - D_{NC})} V_{in} \quad (10)$$

$$V_{ax} = \frac{k D_{NC}}{D'}\left(V_{in} - V_o\right) + (n-1) V_o \,,\; k = \frac{l_{l2}}{L_{11} + L_{22} + 2L_{12}} \quad (11)$$

where L_{11}, L_{22}, and L_{12} are the primary and secondary winding self and mutual inductances, respectively and l_{l2} represents the leakage inductance of the secondary winding.

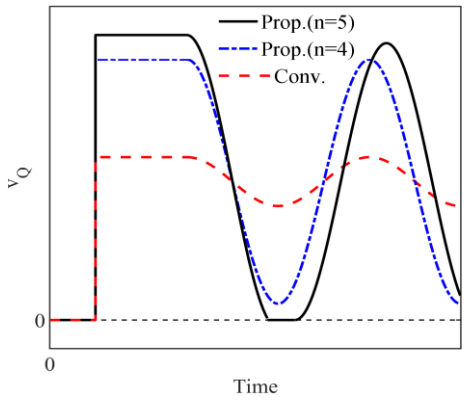

Fig. 7. Theoretical MOSFET output voltage for the conventional and the proposed converter.

D' shows the ratio of falling time of the leakage inductance current to switching period. Note that the leakage inductance value is very smaller than magnetizing inductance, therefore the current caused by secondary leakage inductance is in discontinuous mode.

When the current reaches zero, a resonance is occurred through the circuit involving of input voltage (V_{in}), windings (N_1 and N_2), output voltage (V_o), and the MOSFET output capacitance (C_{oss}). The MOSFET output voltage by neglecting the leakage inductance (l_{l2}) is calculated using (12).

$$v_Q(t) = (V_{in} - V_o) + (n+1)V_o \cos(\omega t) \tag{12}$$

$$\omega = \frac{1}{\sqrt{L_{eq} C_{oss}}}, \; L_{eq} = \left(\frac{n+1}{n}\right)^2 L_m \tag{13}$$

Comparing (1) with (11) indicates that the minimum output voltage of the MOSFET decreases from (V_{in}-2V_o) to (V_{in}-(n+2)V_o). This minimum value can be decreased to zero if (5) is regarded because the reverse body diode of the MOSFET conducts when this voltage tends to be negative. In this condition, zero voltage switching (ZVS) will accompany zero current switching (ZCS) if valley switching activates. Fig. 7 shows the MOSFET output voltage for the conventional and the proposed LED driver for typical elements' value. and for two ratio values of n=4 and n=5. As seen the minimum point of the MOSFET output voltage is zero when the turn ratio is greater than 4. In fact, in this condition the reverse body diode of the MOSFET turns on and the output voltage of the MOSFET is clamped to zero.

IV. Efficiency Comparison

All losses consist of the MOSFET (both for on and off switching losses), inductors and diodes conducting losses are investigated to compare the efficiency of the proposed driver with the conventional buck LED driver. The average output current of the proposed and conventional converters LED drivers should be equal to compare the conducting losses of inductors or diodes. The average output current of the proposed converter in (8) is equal to its value for the conventional in (9), if equation (14) is satisfied.

$$I_{NC\max} = \frac{1}{(D_{NC} + n(1 - D_{NC}))} I_{CC\max} \tag{14}$$

The rms values of output currents for both converters should be calculated as follow to compare the conduction losses.

$$I_{NCrms} = \frac{I_{NC\max}}{\sqrt{3}} \sqrt{D_{NC} + n^2 (1 - D_{NC})} \tag{15}$$

$$I_{CCrms} = \frac{I_{CC\max}}{\sqrt{3}} \tag{16}$$

where I_{NCrms} and I_{CCrms} are the proposed and conventional converter output rms currents, respectively. The rms current value of the proposed LED driver can be achieved as a function of rms current value of the conventional LED driver using (14), (15), and (16).

$$I_{NCrms} = I_{CCrms} \frac{\sqrt{D_{NC} + n^2 (1 - D_{NC})}}{(D_{NC} + n(1 - D_{NC}))}. \tag{17}$$

If the output voltage of the conventional and the proposed converters becomes equal, the relationship between their duty cycle can be achived by (3), and (10).

$$D_{CC} = \frac{D_{NC}}{D_{NC} + (n+1)(1 - D_{NC})} \tag{18}$$

A. MOSFET Switching Losses

While the off state switching loss are the same at two converters, they are different at the on state switching loss. According to (4), the on state switching loss of the MOSFET increases in low voltage applications in conventional converters but it is zero in the proposed LED driver.

B. MOSFET Conduction Losses

Conduction losses depend on the MOSFET rms current and its on state resistance (R_{ON}).

$$P_{NCMcon} = R_{ON} \frac{I_{NC\max}^2}{3} D_{NC} \tag{19}$$

$$P_{CCMcon} = R_{ON} \frac{I_{CC\max}^2}{3} D_{CC} \tag{20}$$

where P_{NCMcon} and P_{CCMcon} are the proposed and conventional MOSFET conduction losses of conventional converter, respectively. The MOSFET conduction loss can be compared using (14), (18), (19), and (20).

$$P_{NCMcon} = M_{CMOS} \times P_{CCMcon}$$
$$M_{CMOS} = \frac{D_{NC} + (n+1)(1 - D_{NC})}{(D_{NC} + n(1 - D_{NC}))^2} \tag{21}$$

Fig. 8 shows coefficient M_{CMOS} versus duty cycle for different turn ratios. As seen, the conduction loss of the MOSFET in new converter is lower than its value for the conventional converter because the coefficient is less than one for all rages of the duty cycle

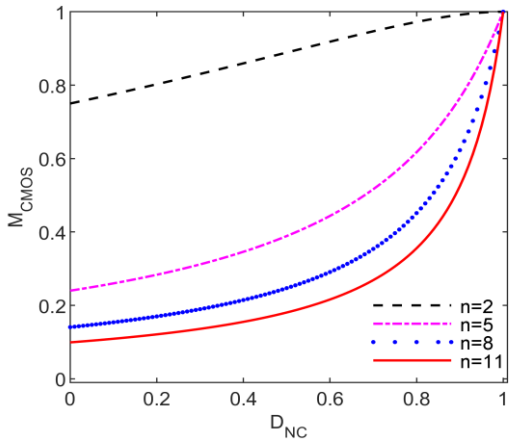

Fig. 8. Coefficient M_{CMOS} versus duty cycle (D_{NC}) for different turn ratios.

C. Inductors Conducting Losses

Resistance of the primary and secondary windings are represented in (22), and (23), respectively.

$$R_p = \frac{1}{n+1} R_w \tag{22}$$

$$R_s = \frac{n}{n+1} R_w \tag{23}$$

where R_p, R_s and R_w are primary, secondary, and total windings resistance, respectively. Primary and secondary winding losses (P_{priw} and P_{secw}) can be calculated using these resistances and their rms current values.

$$P_{priw} = \frac{1}{n+1} R_w \frac{I_{NC\max}^2}{3} \left(D_{NC} + n^2 \left(1 - D_{NC}\right) \right) \tag{24}$$

$$P_{\sec w} = \frac{n}{n+1} R_w \frac{I_{NC\max}^2}{3} D_{NC} \tag{25}$$

Inductor loss of the proposed and conventional LED driver can be calculated using (14), (15), (16), (17), (24), and (25). It can be expressed as:

$$P_{NCLL} = M_L \times P_{CCLL}$$

$$M_L = \frac{1}{n+1} \frac{D_{NC} + n^2 \left(1 - D_{NC}\right) + n D_{NC}}{\left(D_{NC} + n\left(1 - D_{NC}\right)\right)^2} \tag{26}$$

$$P_{CCLL} = R_w I_{CCrms}^2 . \tag{27}$$

where P_{NCLL} and P_{CCLL} are inductor loss of the proposed and conventional converter, respectively. Fig. 9 shows coefficient M_L for different turn ratios. As can be seen, M_L is less than 1; therefore, inductor loss of the proposed converter are less than inductor loss of the conventional converter.

D. Diodes Conducting Losses

As explained in the previous section, only diode D_1 turns on when the MOSFET turns off. Diode loss depends on its forward voltage drop (V_F) and its average current.

$$P_{NCDL} = \frac{1}{2} I_{NC\max} V_F \left(1 - D_{NC}\right) \tag{28}$$

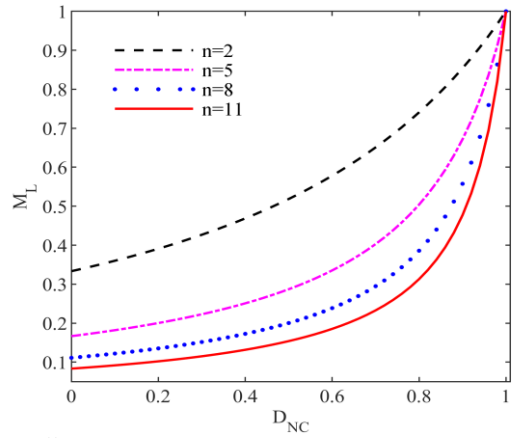

Fig. 9. Coefficient M_L versus duty cycle (D_{NC}).

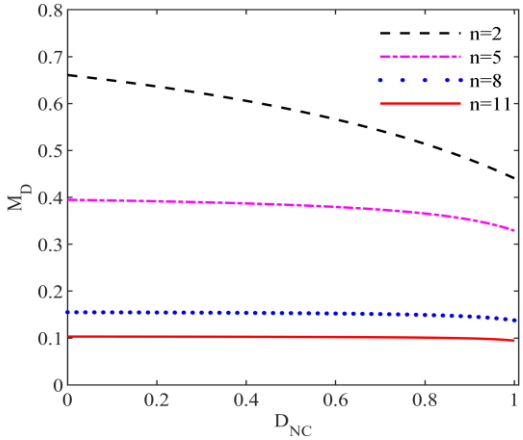

Fig. 10. Coefficient M_D versus duty cycle (D_{NC}).

$$P_{CCDL} = \frac{1}{2} I_{CC\max} V_F \left(1 - D_{CC}\right) \tag{29}$$

where P_{NCDL}, P_{CCDL} are diode losses of the proposed and conventional converters, respectively. It is supposed that the forward voltage of the diode is constant for simplicity. Diode losses can be compared using (14), (18), (28), and (29).

$$P_{NCDL} = M_D \times P_{CCDL}$$

$$M_D = \frac{\left(D_{NC} + \left(n+1\right)\left(1 - D_{NC}\right)\right)}{\left(n+1\right)\left(D_{NC} + n\left(1 - D_{NC}\right)\right)} \tag{30}$$

Fig. 10 shows coefficient M_D for different turn ratios. It shows that the diode loss in the proposed LED driver is less than the conventional diode loss.

V. New Valley Switching Implementation

In the conventional LED drivers a secondary winding is coupled to the converter inductance to implement the valley switching. The minimum point of output voltage of the MOSFET occurs when the slope of voltage across this winding approaches zero. The extra winding causes cost and size of the converter increases. In addition, an extra sensing pin in controller IC is needed [27].

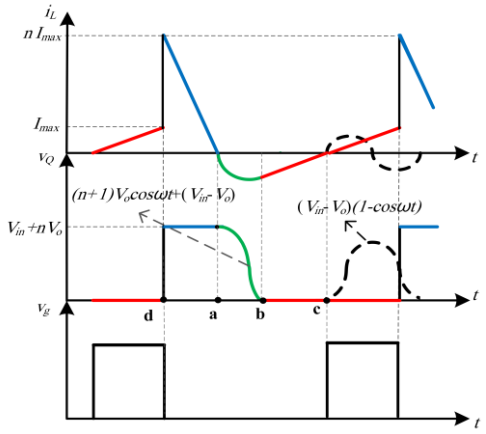

Fig. 11. Theoretical waveform of inductance current, The MOSFET output and gate voltage.

A new method to implement valley switching can be introduced using the proposed converter. Fig. 11 shows the inductance current, the MOSFET output voltage, and the MOSFET gate voltage. In current control mode, the gate pulse becomes zero when the inductance current reaches the reference maximum current (I_{max}). The converter diodes conduct at point **d** after a resonance which is not shown in this figure. Another resonance occurs between the inductor current and the MOSFET parasitic capacitance just the current reaches zero value and diodes turn off (point **a**). The reverse body diode of the MOSFET conducts just the output voltage of the MOSFET tends to be a negative value (point **b**), therefore the inductance current rises from a negative value and the reverse diode turns off when this current becomes positive (point **c**). At this moment, a resonance occurs between the converter inductance and the parasitic output capacitance of the MOSFET.

$$v_Q(t) = (V_{in} - V_o)(1 - \cos(\omega t)),\ \omega = \frac{1}{\sqrt{L_{eq} C_{oss}}} \qquad (31)$$

The next switching should be done at point **c** to implement the zero current switching accompanied by zero voltage switching. The main characteristic of point **c** is that it occurs when the MOSFET output voltage is zero while the gate pulse is zero, too. The next switching point can be done by knowing this fact and should be done just the MOSFET voltage tends to be a positive value. Fig. 12 shows the implementation of this switching method. The output of gate *AND1* goes high when both the MOSFET gate and output voltage become zero. This gate's output after a small delay provides the first input signal of gate *AND2*. This delay is due to preventing switching at point **d**. The output of this gate *AND2* becomes high just the MOSFET output voltage tends to be a positive value (point **c**). Consequently, the output of flip-flop becomes high and the MOSFET turns on at this point. Many converter IC controllers in current control mode have separated synchronizing pin or can do synchronization using oscillation pin. The output signal of *AND2* can be connected to synchronizing pin and the output signal of current comparator (*Cp*) can supply the current control pin of these ICs; therefore, the extra sensing pin is not required.

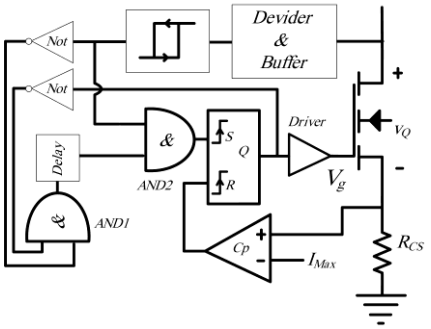

Fig. 12. The new valley switching.

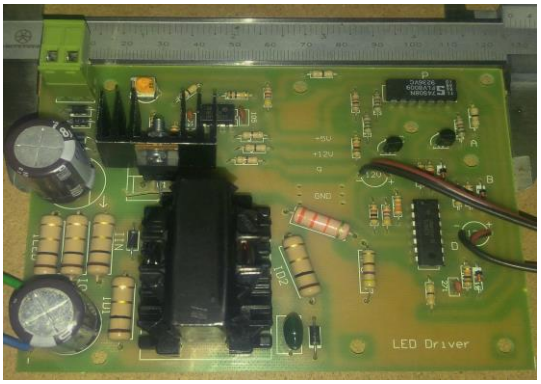

Fig. 13. Experimental setup.

VI. Experimental Results

Fig. 13, and Fig. 14 show the experimental setup used to implement the proposed LED driver. A 15W/33V LED lamp is used as output load and UC3844 converter controller is used in current control mode. This IC uses oscillation pin (pin 4) for synchronization. The current feedback is implemented by a resistor connected to the source pin of the MOSFET. Other specifications are shown in table I. The input and output voltage values are 310V and 33V, respectively, therefore the primary and secondary winding numbers are 27 and 166 turns, respectively. Fig. 15 shows the current waveform of the proposed and conventional converters when the valley switching is implemented. It verifies the theoretical waveform of Fig. 6 and there is no voltage oscillation because the on switching state occurs at the minimum point of the MOSFET output voltage.

TABLE I
SYSTEM PARAMETERS

Parameter	Description	Value
MOSFET	The main switch	IRF840
IC Controller	Converter controller IC	UC3844
N_1	Primary winding	27
N_2	Secondary winding	166
C_o	Output capacitor	10uF,400V
C_{ax}	Auxiliary capacitor	820PF,1200V
C_{in}	Input capacitor	68uF,400V
D_1	Primary winding diode	UF4007
D_2	Secondary winding diode	UF4007
R_{cs}	Current feedback resistor	1Ω,1W
R_G	The MOSFET gate resistor	33Ω,0.25W

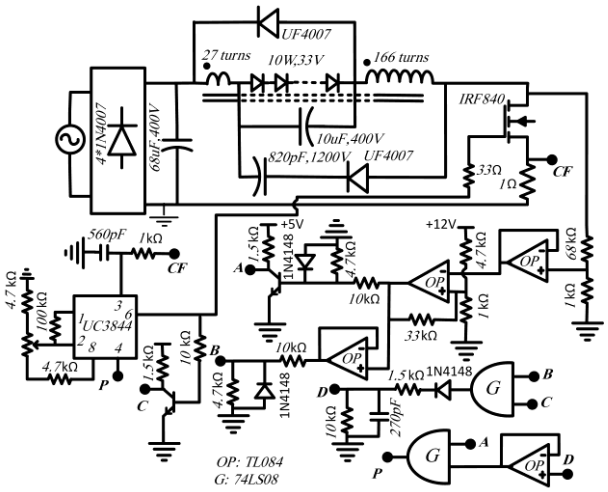

Fig. 14. LED driver circuit.

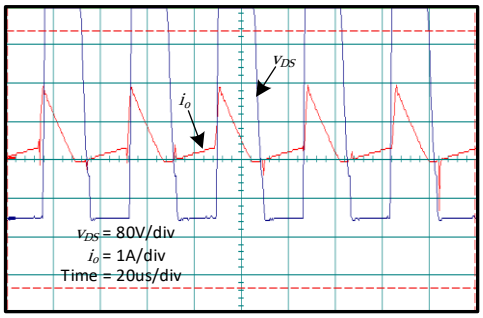

Fig. 15. Drain to source voltage of the MOSFET and output current.

Valley switching can be disabled to show the MOSFET output voltage oscillations in the proposed LED driver. Fig. 16 shows the output voltage of the MOSFET for the proposed LED driver when the valley switching is not performed and the converter works in DCM mode. As seen, the minimum point of the output voltage approaches near zero in the proposed circuit, therefore if the valley switching is activated, the switching losses will be much smaller than the conventional converter.

The losses of LED driver elements including losses in inductance, diode, and the MOSFET for the proposed and conventional LED driver are calculated at the same working conditions using (3), (9), (14), and (18) and are shown in Table II. Fig. 17 illustrates the losses of converter elements consist of inductance, diode, and the MOSFET for the proposed and conventional LED driver. It can be seen in this figure that the losses of the proposed circuit are much smaller than their values for the conventional LED driver.

TABLE II
WORKING CONDITION

Parameter	Description	Value
I_o	Output current	450 mA
I_{CCmax}	I_{max} for the conventional LED driver	900 mA
I_{NCmax}	I_{max} for the proposal LED driver	241 mA
D_{CC}	Duty cycle of the conventional LED driver	0.105
D_{NC}	Duty cycle of proposal LED driver	0.455

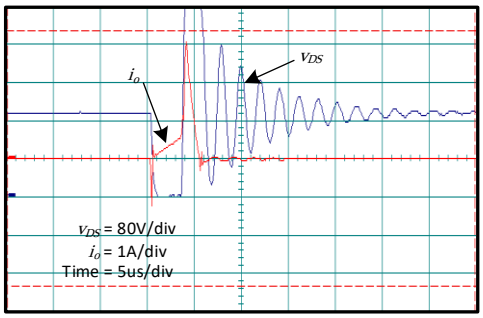

Fig. 16. Drain to source voltage of the MOSFET and output current for proposed converter when valley switching is disabled.

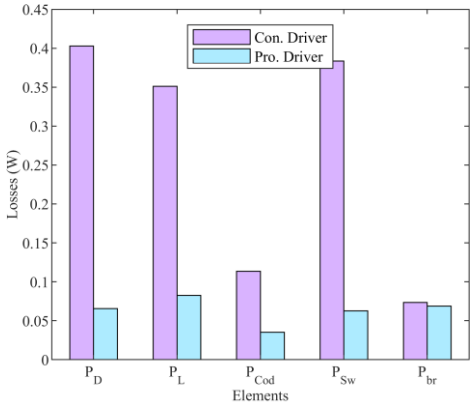

Fig. 17. Losses of converter elements. P_D: converter diodes losses, P_L: inductance losses, P_{Cond}: MOSFET conduction losses, P_{Sw}: MOSFET switching losses, P_{br}: diode bridge losses.

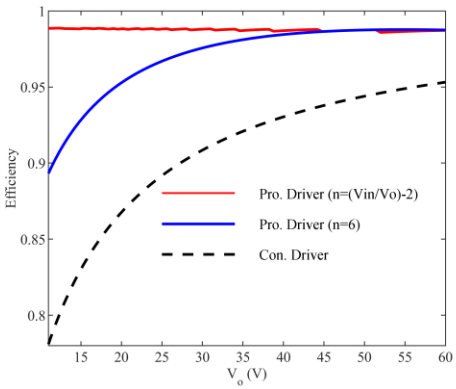

Fig. 18. The proposed and conventional converter efficiency.

In this condition, the efficiency of the proposed LED driver is 98% while the efficiency of the conventional LED driver is 92%. Fig. 18 shows the efficiency of the proposed and conventional converters as a function of output voltage. The input voltage values are set 310 volts and the windings turn ratio is regarded 6 and using (4). As seen, the efficiency of the conventional LED driver is lower than the proposed LED driver for the range of output voltage. In addition, at lower range of output voltage, the difference between two LED drivers' efficacy is even more significantly. As an example, at

output voltage equal to 10V, the efficiency of the proposed LED driver is 97%, and 89% for turn ratio achived by (5), and n=6, respectively, while it is only 78% in the conventional converter.

VII. Conclusions

In this study, a new buck LED driver is introduced to improve its efficiency. By elaborating the proposed driver configuration and analyzing power losses of main elements (i.e. the MOSFET, inductors, and diodes) it is shown that at the same operating conditions, the proposed LED driver has much more higher efficiency than the conventional one. The reason is based on two principles. Firstly, the minimum point of output resonant voltage of the MOSFET is near zero in the proposed LED driver, therefore the the switching loss of the MOSFET decreases dramatically using valley switching method. This result is more prominent when the output voltage value is very lower than the input voltage value. The secondely, is the current waveform of the proposed LED driver is changed in a way that the other main losses consist of the MOSFET, inductance, and diode conduction losses are reduces strongly. Also, a new valley switching method is introduced according to the new converter which does not require the coupling winding. Therefore, the cost and dimension of the proposed converter is much less than the conventional driver.

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